What is claimed is:

1. A computer system comprising:

a plurality of memory slots each of which has a structure for accepting a memory module inserted therein and includes a plurality of connector terminals for being in contact with module pins formed in said memory module;

a memory bus which includes a plurality of signal lines coupled to the at least one connector terminal of each of said plurality of memory slots;

a memory controller which is coupled to a plurality of memory chips on said memory module inserted in at least one of said plurality of memory slots, through said memory bus; and

at least one electric load, and wherein

said plurality of memory slots includes

a first part of memory slots which is coupled to said memory module and provides electrical contact between the plurality of signal lines of said memory bus and the module pins, respectively, using their corresponding connector terminals, and

a second part of memory slots which is not coupled to said memory module and provides electric contact between the plurality of signal lines of said memory bus and the electric load using their corresponding connector terminals.

2. The computer system according to claim 1, wherein

impedance of the electric load is approximately equal to impedance of said memory module.

3. The computer system according to claim 1, wherein

the electric load is at least one series circuit including a resistance device and a capacitive device or at least one capacitive device.

4. The computer system according to claim 3, wherein:

the resistance device is a variable resistor; and/or

the capacitive device is a variable capacitor.

5. A computer system comprising:

a plurality of memory slots each of which has a structure for accepting a memory module inserted therein and includes a plurality of connector terminals for being in contact with module pins formed in said memory module;

a memory bus which includes a plurality of signal lines coupled to at least one of said plurality of connector terminals of each of said plurality of memory slots;

a memory controller which is coupled to a plurality of memory chips on said memory module inserted in at least one of said plurality of memory slots, through said memory bus; and

a plurality of electric loads, and wherein:

said plurality of connector terminals included in each of said plurality of memory slots includes

a first-type connector pin which is coupled to one of said plurality of signal lines of said memory bus, and

a second-type connector pin which is coupled to a corresponding one of said plurality of electric loads;

said first-type connector pin and said second-type connector pin are electrically in contact with each other, in a case where the memory module is not inserted in each of said plurality of memory slots; and

said first-type connector pin and said second-type connector pin are electrically insulated from each other, and the first-type connector pin and said module pins of said memory module are electrically in contact with each other, in a case where the memory module is coupled to each of said memory slots.

6. The computer system according to claim 5, wherein

impedance of each of said plurality of electric loads is approximately equal to impedance of said memory module.

7. The computer system according to claim 5, wherein

each of said plurality of electric loads is at least one series circuit including a resistance device and a capacitive device or at least one capacitive device.

8. The computer system according to claim 7, wherein:

said resistance device is a variable resistor, and/or

said capacitive device is a variable capacitor.

9. A switch connector which is adaptable to a computer system including, a memory bus, at least one memory slot and an electric load, wherein:

said switch connector couples one of a plurality of signal lines of said memory bus to one of a plurality of module pins of a memory module, in a case where said memory module is inserted in said at least one memory slot; and

said switch connector couples the one of said plurality of signal lines of said memory bus to said electric load, in a case where said memory module is not inserted in said at least one memory slot.

10. The switch connector according to claim 9, wherein

said switch connector is disposed inside said at least one memory slot.

11. A switch connector which is adaptive to a computer system including, a memory bus, at least one memory slot and an electrical load, comprising:

a first connector pin which is coupled to one of a plurality of signal lines of said memory bus; and

a second connector pin which is coupled to said electric load, and wherein

said switch connector provides electric contact between said first connector pin and said second connector pin, in a case where a memory module is not inserted in said at least one memory slot, and

said switch connector insulates said first connector pin from said second connector pin, in a case where said memory module is not inserted in said at least one memory slot.

12. The switch connector according to claim 11, wherein:

one end of said first connector pin is fixed on a casing of said at least one memory

slot; and

other end of said first connector pin provides flexible electric contact with said second connector pin or with one of a plurality of module pins of said memory module.

13. A method of controlling operations of a computer system including a plurality of memory slots, comprising:

arranging a plurality of memory connectors on each of said plurality of memory slots;

coupling a plurality of bus lines respectively to said plurality of memory connectors;

coupling at least one impedance matching circuit to at least one of said plurality of memory connectors;

coupling said plurality of bus lines to a memory module, in at least one of said plurality of memory slots in which the memory module is inserted; and

coupling said at least one impedance matching circuit to at least one of said plurality of bus lines, in at least one of said plurality of memory slots in which the memory module is not inserted.

14. The method according to claim 13, further comprising:

coupling said plurality of bus lines respectively to first-type connector pins included in each of said plurality of memory connectors;

coupling said at least one impedance matching circuit to at least one of second-type connector pins included in at least one of said plurality of memory connectors;

providing electric contact between said first-type connector pins and module pins of the memory module, in the at least one of said plurality of memory slots in which the memory module is inserted; and

providing electric contact between said first-type connector pins and said second-type connector pins, in at least one of said plurality of memory slots in which the memory module is not inserted.